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TECHNOLOGY UTILIZATION

ELECTRONIC AMPLIFIERS

CASE FILE COPY

A COMPILATION



NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Foreword

The National Aeronautics and Space Administration and the Atomic Energy Commission have established a Technology Utilization Program for the dissemination of information on technological developments which have potential utility outside the aerospace and nuclear communities. By encouraging multiple application of the results of their research and development, NASA and AEC earn for the public an increased return on the investment in aerospace research and development programs.

The innovations in this updated series of compilations dealing with electronic circuits represent a carefully selected collection of items on electronic amplifiers. Most of the items are based on well known circuit design concepts that have been simplified or refined to meet demanding requirements for reliability, simplicity, safety, and environmental adaptability. The items included in the six sections should be of particular interest to the electronic technician and hobbyist.

Additional technical information on individual devices and techniques can be requested by circling the appropriate number on the Reader Service Card included in this compilation.

Unless otherwise stated, NASA and AEC contemplate no patent action on the technology described.

We appreciate comment by readers and welcome hearing about the relevance and utility of the information in this compilation.

Ronald J. Philips, *Director*
Technology Utilization Office
National Aeronautics and Space Administration

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Contents

	Page
SECTION 1. Preamplifiers with Wide Dynamic Range	
Miniature Electrometer Preamplifier Effectively Compensates for Input Capacitance	1
SiC/Si Diode Trigger Circuit Provides Automatic Range Switching for Log Amplifier	1
Tiny Biomedical Amplifier Combines High Performance, and Low Power Drain	2
Log Amplifier Instrument Measures Physiological Biopotentials Over Wide Dynamic Range	3
Magnetometer Preamplifier	4
Transistor Circuit Increases Range of Logarithmic Current Amplifier	4
SECTION 2. High Power Amplifiers	
Wideband Power Amplifier	5
Single-Transistor Circuit Boosts Pulse Amplitude	5
Microelectronic Power Amplifier	6
SECTION 3. Communications Systems Amplifiers	
Gain and Phase-Tracking Amplifier	6
130 MHz AGC Amplifier	7
Low Noise Wide-Bandwidth IF Preamplifier	7
Variable Gain Amplifier	8
Complementary Pair Broadband Transistor Amplifier	9
SECTION 4. Buffer and Isolation Amplifiers	
Buffer Amplifier Provides Inverted and Non-Inverted Outputs	10
Field Effect Transistors Improve Buffer Amplifier	11
AC-Coupled Ultrahigh Input Impedance Amplifier	11
Amplifier Provides Dual Outputs from a Single Source with Complete Isolation	12
Signal Conditioner, Isolation Attenuator	12
SECTION 5. Amplifier Circuits for Increased Reliability	
Circuit Provides Overcurrent Protection to Push-Pull Amplifier	13
Ground Equalizer Amplifier	14
Continuous Redundancy DC Amplifiers	15
Amplifier Gain Control	15
Self-Check Circuits for AC and DC Amplifiers	16
Amplifier Corrects Errors Introduced by Large Spurious Input Signals	17

SECTION 6. General Purpose Amplifiers

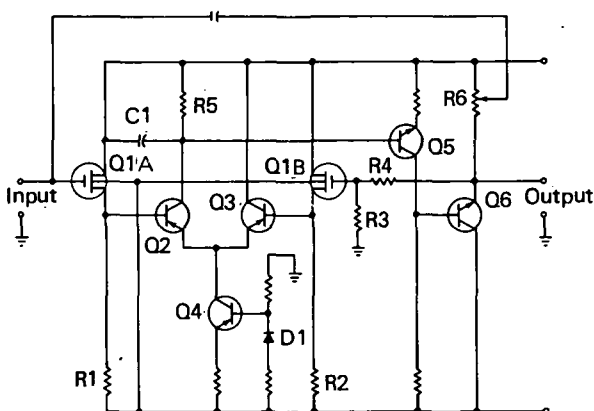
Low Power Bias and Erase Circuit for Magnetic Tape Recorders	18
Input Gate Circuit Converted for Use as a Linear Amplifier	19
Improved Compensation Circuit for Direct-Coupled Amplifiers	20
Signal Conditioner, DC Amplifier	20
Stable Amplifier Has High Common-Mode Rejection	21
General Purpose FET Amplifier with High Gain and Low Distortion	22

Section 1. Preamplifiers with Wide Dynamic Range

MINIATURE ELECTROMETER PREAMPLIFIER EFFECTIVELY COMPENSATES FOR INPUT CAPACITANCE

This preamplifier can be used wherever stable wideband dc amplification from high impedance sources is required. Typical applications include biomedical instrumentation, video amplifiers, and pH and ionization chambers.

An exceptionally high input impedance is achieved with the use of a dual MOS transistor in the input stage. The input signal is coupled to the gate of Q1A which is one-half of the dual MOS transistor employed in a differential amplifier configuration. Temperature compensation is achieved automatically since both Q1A and Q1B are diffused on a single substrate. Open-loop gain is provided by Q2, Q3, and Q5. Resistors R1 and R2 determine the drain currents and are selected so that the temperature coefficient of the gate-to-source voltage is approximately zero. R3 and R4 form a 2:1 negative feedback potential divider which determines the closed-loop gain. R5 shunted by C1 provides the stability necessary to prevent the circuit



from oscillating. The negative capacitance control, determined by the setting of R6, can be reduced to less than 1.0 pF.

Source: G. J. DeBoo and C. N. Burrows
Ames Research Center
(ARC-69)

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SiC/Si DIODE TRIGGER CIRCUIT PROVIDES AUTOMATIC RANGE SWITCHING FOR LOG AMPLIFIER

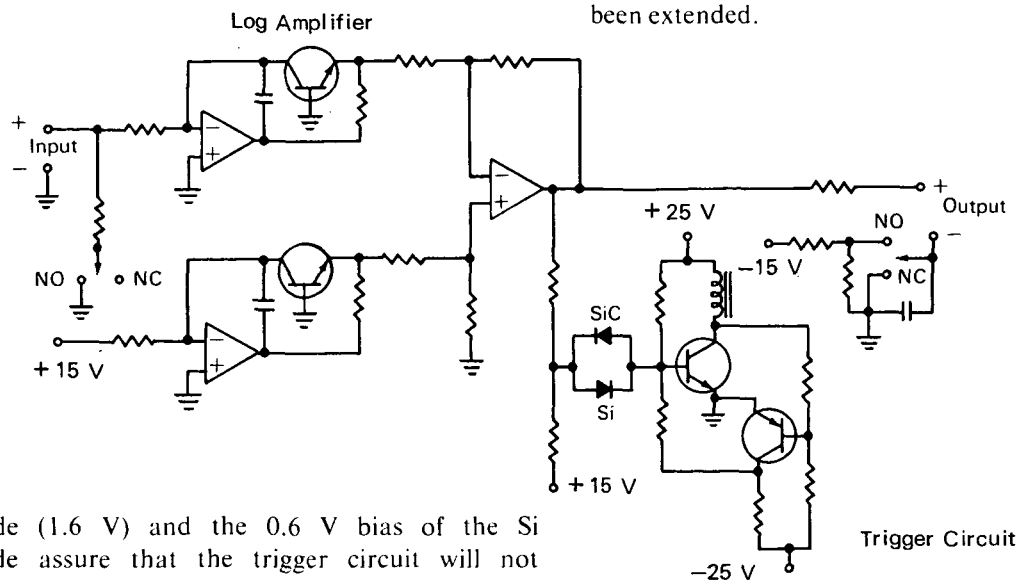
An automatic ranging circuit extends the operating range of a logarithmic amplifier and increases its stability near the range switch-over point. A silicon carbide (SiC) and silicon (Si) diode pair provide hysteresis (bias voltage offset) for a trigger circuit that actuates a relay at the desired range extension point. A trigger circuit, consisting of a transistor-driven relay, provides the range extension, while the diode

pair provides the voltage offset and increases the stability.

If no hysteresis were provided at the input to the trigger circuit, any noise associated with the input current at or very near the range switchover point would cause the extender circuit to drop in and out on each noise spike. To avoid this instability, the SiC diode is placed in parallel with the Si diode to provide

the voltage offset at the input to the trigger circuit. The forward bias voltage drop of the SiC

appropriate voltage at the output to cover the number of decades the system range has been extended.



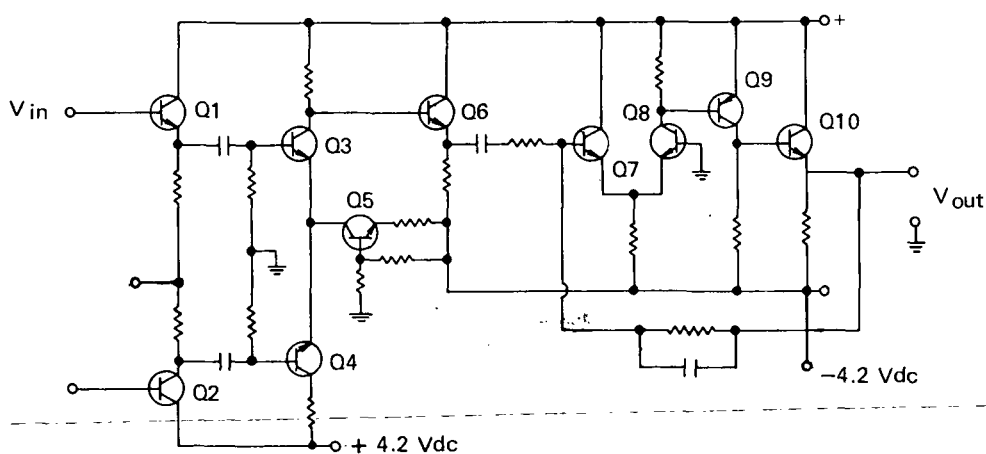
diode (1.6 V) and the 0.6 V bias of the Si diode assure that the trigger circuit will not energize and deenergize at precisely the same input current.

Although this system provides a range extension of two decades, any desired decade extension can be obtained by selecting the division factor of the input circuit, and adding the

Source: Tyco Laboratories
under contract to
Marshall Space Flight Center
(MFS-1879)

Circle 2 on Reader Service Card.

TINY BIOMEDICAL AMPLIFIER COMBINES HIGH PERFORMANCE AND LOW POWER DRAIN



A tiny, high-performance amplifier utilizes a differential input to obtain a common-mode rejection of 25,000 to 1. Because of its small

size and low power drain, it could be used in the biomedical field for amplifying electrocardiogram and electromyogram signals and

could be mounted directly on an ambulatory subject.

Emitter follower transistors Q1 and Q2 provide the necessary high input impedance of about 10 M Ω . The differential output of the emitter followers is converted to a single-ended signal by a difference amplifier consisting of Q3, Q4, and Q5. Q5 provides the difference amplifier with the high emitter impedance necessary for high common-mode rejection. The signal is fed sequentially through emitter follower Q6, a second difference amplifier Q7 and Q8, a common emitter amplifier Q9, and a final emitter

follower Q10. Capacitance coupling in these stages is minimized to provide good low frequency response from 0.15 Hz. The amplifier exhibits a gain of 1,000 while drawing 5 mW of power. This amplifier has been constructed in a weld-connected cordwood configuration having dimensions of 2.0 cm by 1.7 cm by 0.9 cm and weighing 4.5 grams.

Source: T. B. Fryer and G. J. Deboo
Ames Research Center
(ARC-41)

Circle 3 on Reader Service Card.

LOG AMPLIFIER INSTRUMENT MEASURES PHYSIOLOGICAL BIOPOTENTIALS OVER WIDE DYNAMIC RANGE

The extreme dynamic range of biopotentials usually exceeds the capability of most recording devices. The electronic amplifier shown in the

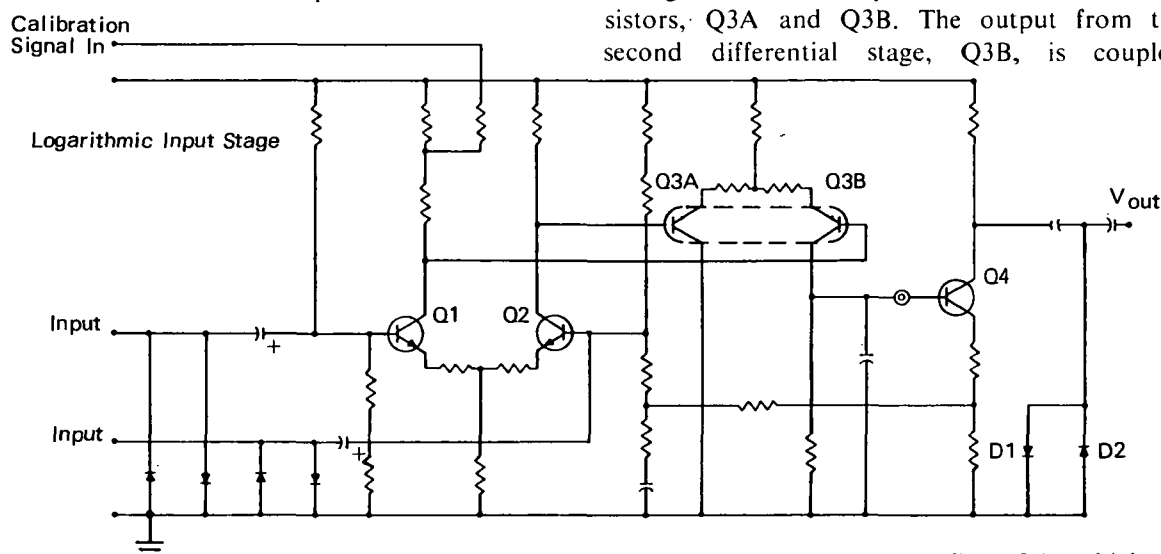


figure compresses the signal amplitudes without resolution loss so that EEG signals can be transmitted. The biopotential inputs are capacitatively coupled to the miniature, low power, solid-state signal conditioner which consists of a two-stage differential preamplifier with a low noise figure.

The differential input stage is a conventional circuit employing two low-noise NPN transistors, Q1 and Q2, with capacitatively coupled inputs and appropriately placed diodes to suppress voltage overloads. The input resistance of

the stage is 1 M Ω . The input transistors are direct-coupled to a difference amplifier consisting of a matched pair of silicon PNP transistors, Q3A and Q3B. The output from the second differential stage, Q3B, is coupled

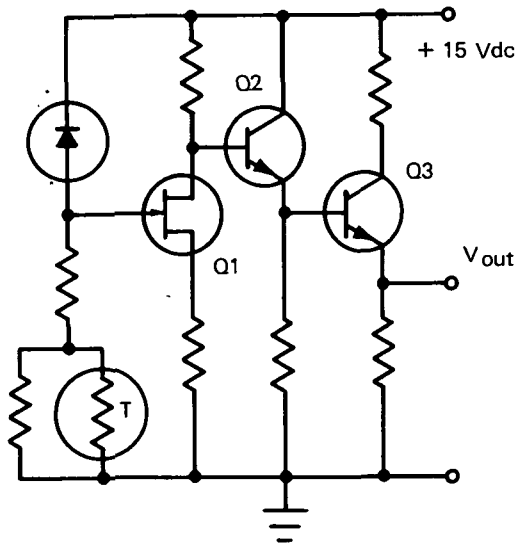
directly to an NPN amplifier, Q4, which in turn provides dc feedback to the base of Q2 for stabilization of the overall amplifier, and feeds an amplified signal via a capacitor to the logarithmic diode signal compressors, (D1 and D2).

Source: R. T. Kado of
University of California at Los Angeles
under contract to
Ames Research Center
(ARC-10032)

Circle 4 on Reader Service Card.

MAGNETOMETER PREAMPLIFIER

The preamplifier, packaged as a thick-film hybrid circuit, is intended for use in a magnetometer, where the stray dc field must be extremely low and all materials must be nonmagnetic.



Fabrication techniques allow miniaturization, and the planar layout simplifies compensation of stray dc fields.

The preamplifier circuit has a high input impedance suitable for operation with a silicon photodiode. The low output impedance (achieved by the emitter-follower Q3) can be matched to drive up to 30 cm of coaxial cable. The preamplifier stage, consisting of Q1 and Q2, has a 3 dB bandwidth of 15 MHz when driven from a low source impedance.

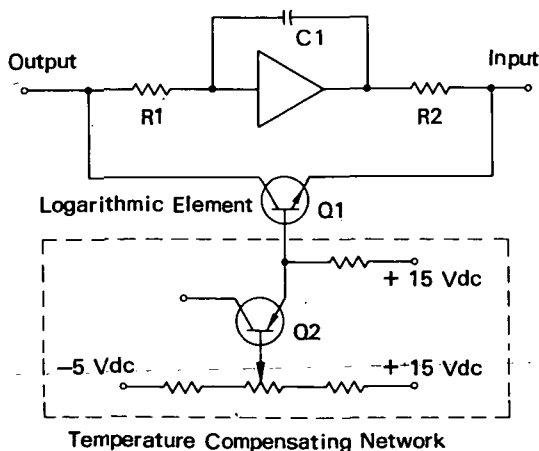
With proper choice of input resistor and photodiode, the circuit can be used as a low gain photodiode preamplifier at frequencies up to 15 MHz.

Source: P. A. Sedalis of
Philco-Ford Corporation
under contract to
Goddard Space Flight Center
(GSC-10931)

Circle 5 on Reader Service Card.

TRANSISTOR CIRCUIT INCREASES RANGE OF LOGARITHMIC CURRENT AMPLIFIER

The logarithmic current amplifier shown in the figure is capable of operating throughout a range of 10^{-10} to 10^{-2} A. The amplifier is



simple to operate and the calibration procedure is straightforward. The wide dynamic amplification range is achieved by placing a logarithmic element in a feedback loop across the amplifier, causing the output voltage to be proportional to the log of the input current. C1 provides circuit stabilization and Q2 provides temperature compensation for Q1. The high input impedance ($10\text{ M}\Omega$) makes the amplifier well suited for applications with electrometers and ionization chambers.

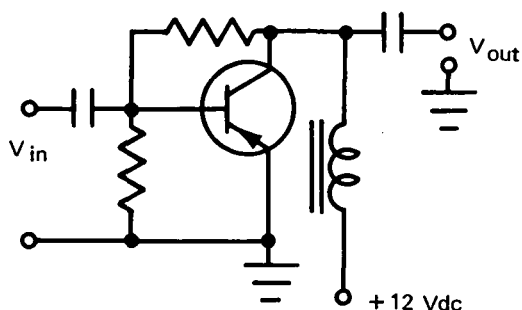
Source: G. Gilmour of
Westinghouse Astronuclear Laboratory
under contract to
Space Nuclear Systems Office
(NUC-00018)

Circle 6 on Reader Service Card.

Section 2. High Power Amplifiers

WIDEBAND POWER AMPLIFIER

An economical power switching transistor can be used in a 5 W power amplifier that has a frequency response from 0.10 to 15 MHz.



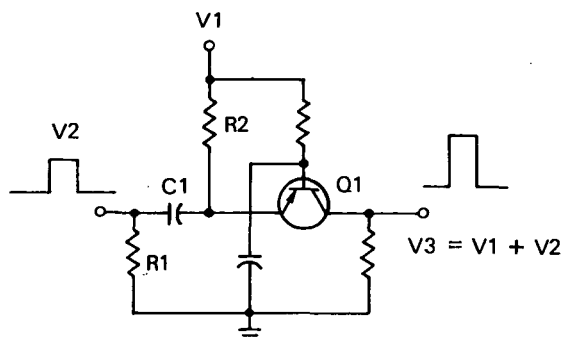
This amplifier should find application in test and calibration operations where an inexpensive method of increasing power output is required. Thirty dB of power gain can be achieved with the simple circuit shown in the schematic.

Source: R. E. Calhoun of
North American Rockwell Corp.
under contract to
Manned Spacecraft Center
(MSC-13058)

Circle 7 on Reader Service Card.

SINGLE-TRANSISTOR CIRCUIT BOOSTS PULSE AMPLITUDE

A simple amplifier circuit provides a voltage pulse greater than that normally available from emitter follower circuits to drive a 100 W trans-



mitter. Capacitor storage, followed by common-base switching, is accomplished with only one transistor.

During circuit operation, capacitor C1 is charged through R1 and R2 to the supply line voltage V1. With no input signal, the emitter and base of the transistor are at the

same potential and the collector is cut off. With an input pulse V2 present, the potential of C1 with respect to ground is increased by V2. The emitter becomes more positive than the base, and the transistor is switched on. This action produces an output pulse, V3, equal to $V1 + V2$ (minus small losses in C1 and the transistor).

In order for C1 to reach approximate full charge between pulses, the ratio of charge interval to charge time-constant must be much greater than the ratio of discharge interval to discharge time-constant. The circuit produces an output waveform at about twice the amplitude of the supply line voltage V1.

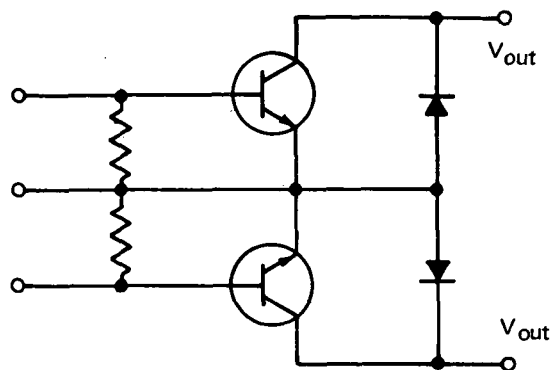
Source: M. W. Matchett and T. Keon of
Cutler Hammer
under contract to
Goddard Space Flight Center
(GSC-501)

Circle 8 on Reader Service Card.

MICROELECTRONIC POWER AMPLIFIER

The power amplifier shown in the figure can serve as a prototype for the volume production of push-pull power transistors for switching or amplifying. The design provides flexibility for scaling either upward or downward, depending on the power dissipation requirements.

The integrated push-pull power amplifier is fabricated on a single chip of silicon. The interdigitated power transistors occupy 80 percent of the area, with the remaining 20 percent being occupied by the resistors and diodes. The device is hermetically encapsulated in a beryllia flat package. Beryllia was chosen over other ceramics because of its high thermal conductivity, high electrical resistivity, and high dielectric strength. Although the amplifier can provide an output of 10 A from an input current drive of 1A, it is capable of current outputs several times greater than the rated value.



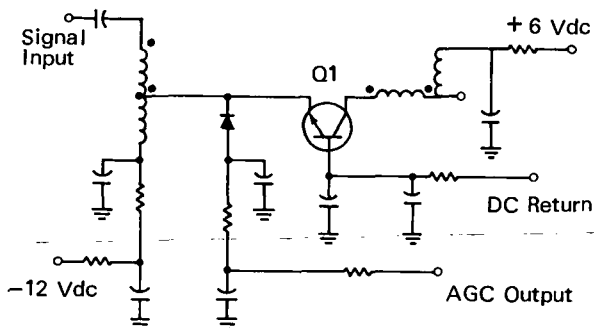
Source: T. C. New of
Westinghouse Electric Corporation
under contract to
Marshall Space Flight Center
(MFS-13621)

Circle 9 on Reader Service Card.

Section 3. Communications Systems Amplifiers

GAIN AND PHASE-TRACKING AMPLIFIER

A comprehensive analysis of IF amplifiers operating at 40.8 MHz was undertaken to provide criteria for selecting the appropriate matched transistors. With the use of matched



transistors, the adverse effects in a common-base amplifier stage are minimized. Included in this analysis is a mathematical model of the AGC circuit shown in the figure. The optimum AGC control voltage was determined, and mathematical expressions were derived to enable the design engineer to select devices for optimum circuit performance.

Source: Herbert L. Slade of
Radio Corp. of America
under contract to
Manned Spacecraft Center
(MSC-12277)

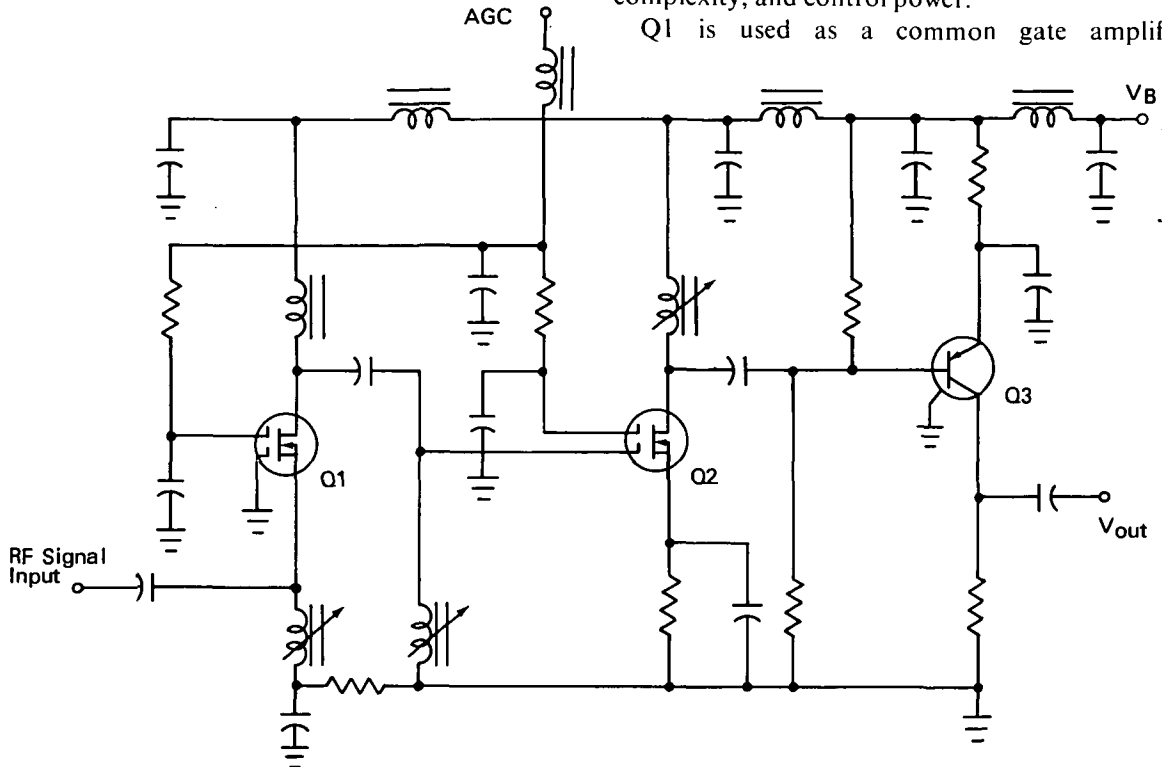
Circle 10 on Reader Service Card.

130 MHz AGC AMPLIFIER

The amplifier shown can be used as the first IF stage in a communication receiver requiring a 50 Ω interface between it and the AGC stage. These receivers are required to handle high in-

cost considerably. The common-base dual-gate MOSFET replaces complex diode attenuators preceding or between fixed-gain stages below 250 MHz, with a substantial savings in cost, complexity, and control power.

Q1 is used as a common gate amplifier



put levels on the order of -4 dBm at the input of the first stage. The amplifier is designed to provide gains of 18 to -34 dBm while maintaining an output level of -40 dBm with a minimum bandwidth of 30 MHz. The ability to apply 200 mV RF signals directly to the input of the first stage is achieved with the use of a dual-gate FET (Q1). The application of the FET in place of conventional diode attenuators simplifies the circuit design and reduces the

for the purpose of simplification, and Q2 is a common source. Q3 provides a ground referenced 50 Ω output source.

Source: R. Rheinlander of
Motorola Inc.
under contract to
Manned Spacecraft Center
(MSC-12290)

Circle 11 on Reader Service Card.

LOW NOISE, WIDE-BANDWIDTH IF PREAMPLIFIER

A comprehensive analytical evaluation of circuit configurations, in terms of optimum overall wideband performance, resulted in the development of a wideband IF preamplifier,

shown in the figure, which can be used in most types of communications receivers. Its exceptional performance features include a 20 dB power gain over the passband of 10 MHz to

100 MHz, with a passband ripple of 1 dB. During the initial design, the major problems which hindered the achievement of a high passband with a concurrent low noise figure were found to stem from the difficulty of achieving a source admittance that was

the noise figure of 1.5 dB at 60 MHz if the passband is from 20 to 120 MHz. The shunt-C, series-L input matching network was found to provide better overall performance from 10 to 110 MHz but had a marginal noise figure.

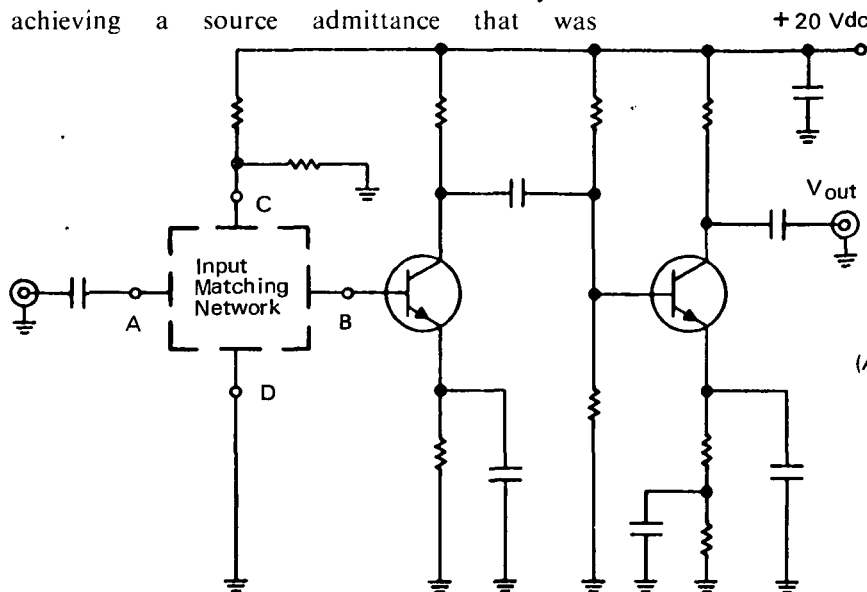


Figure 1A Two-Stage Amplifier

optimum with respect to the noise figure over a wide bandwidth.

After a thorough analytical investigation, the basic configuration chosen was a two-stage, common-emitter amplifier with series feedback in the second stage only (see fig. 1A). The design in Fig. 1B provides a choice between the two input matching networks (A and B) that optimize performance over different portions of the passband. Further computer analysis showed that the simple, shunt-L network meets

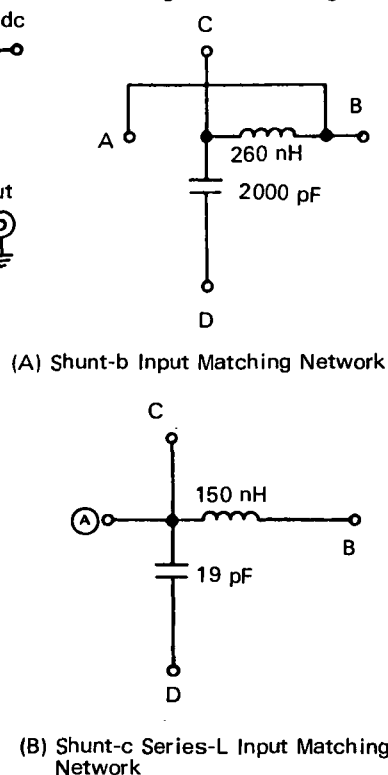


Figure 1B

Source: W. S. Jones and G. R. Pierson of Texas Instruments under contract to Electronic Research Center (ERC-10321)

Circle 12 on Reader Service Card.

VARIABLE GAIN AMPLIFIER

The design of this amplifier combines improved input and output impedances with relatively large signal handling capability and an immunity from the usual adverse effects of automatic gain control (AGC). These advantages are achieved through the use of two FETs, with sources and drains in parallel, plus a resistive

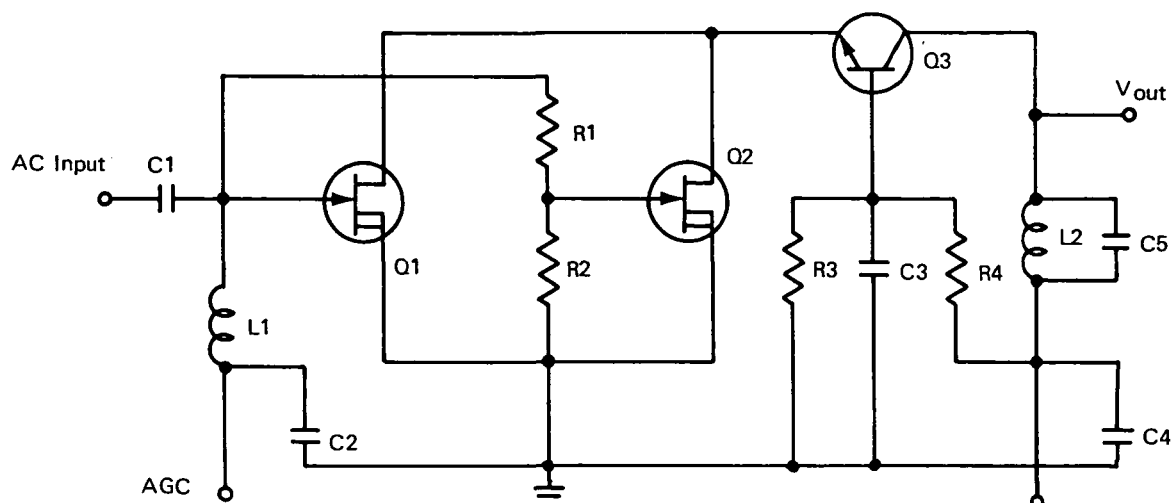
divider for the signal, and bias to either of the gate terminals.

The ac signal is coupled into the circuit with C1, L1 provides a high impedance to the ac signal and a low impedance path for the AGC potential, while C2, C3, and C4 (bypass capacitors) provide low impedance ac-signal paths. R1

and R2 divide the ac signal and AGC potential applied to the gate of Q1, and L2 and C5 form a tuned resonant circuit which is the load impedance at the ac operating frequency. The two FETs, Q1 and Q2, with their drains and sources in parallel, and their gates tied together through

Since the signal is divided by the resistors, larger signals may be used as Q2 approaches cutoff for the same amount of distortion in the drain current.

The grounded-base configuration of Q3 provides a low impedance drain load for Q1



the resistive-divider R1 and R2, produce the remote cutoff feature that makes the circuit perform in a manner similar to that of a remote-cutoff vacuum tube. At low values of AGC bias, both Q1 and Q2 contribute to the forward transfer admittance. Since the signal is attenuated, Q2 does not contribute as much to the forward transfer admittance under low values of AGC bias as Q1 does. As the bias is increased, Q1 approaches cutoff more rapidly than Q2 because the bias applied to Q2 is also divided by R1 and R2. As Q1 approaches cutoff, Q2 takes over control of the forward transfer admittance of the circuit. The AGC bias required to cutoff Q2 is larger than that required to cutoff Q1 by a factor determined by R1 and R2. With the proper selection of the ratio of R1 and R2, the FET transfer characteristic can be optimized for a smooth transition.

and Q2. This further reduces the reverse energy transfer from drain-to-gate of Q1 and Q2, and therefore reduces input impedance variations produced by the AGC.

This reduction is important, because input impedance variations (as a function of AGC voltage) are virtually eliminated. This feature is especially important in RF and IF amplifiers where input impedance variations can alter the bandwidth and center frequency of the previous stage. The output impedance of Q3 remains high and minimizes the variation in damping across the load tuned circuit.

Source: G. H. Spaid
Goddard Space Flight Center
(GSC-10116)

Circle 13 on Reader Service Card.

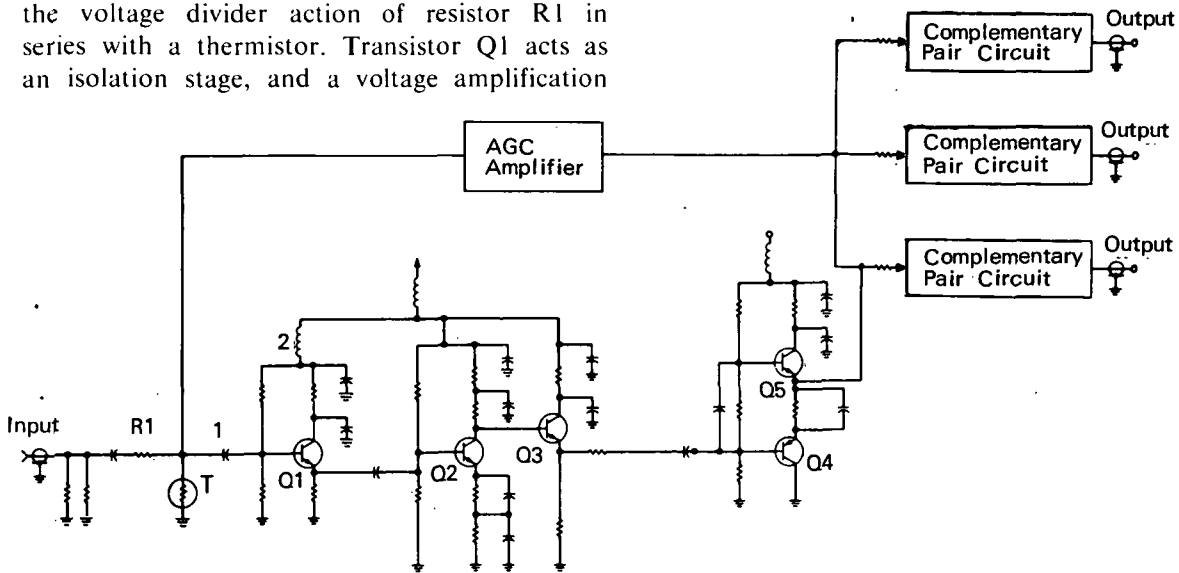
COMPLEMENTARY PAIR BROADBAND TRANSISTOR AMPLIFIER

A wideband distribution amplifier with a bandwidth of 50 MHz can be used in commercial radio, FM and television circuits. Additional

applications may include its use in pulse and timing circuitry in computers.

In operation, the input signal is attenuated by

the voltage divider action of resistor R1 in series with a thermistor. Transistor Q1 acts as an isolation stage, and a voltage amplification



of 10 is achieved by the next stage, which includes Q2. The signal is then fed into a high-impedance emitter follower Q3.

The complementary pair of transistors, Q4 and Q5, functions as a driver for the final output stages. The output impedance of the complimentary emitter follower output stages is very low, allowing them to drive low impedance loads with low distortion.

Since the basic amplifier is a linear device, an automatic gain control (AGC) system is

required; 20 dB of AGC is obtained by varying the resistance of the thermistor in the attenuator circuit.

Source: G. D. Thomson, Jr. and
G. F. Lutes, Jr. of
Caltech/JPL
under contract to
NASA Pasadena Office
(NPO-10003)

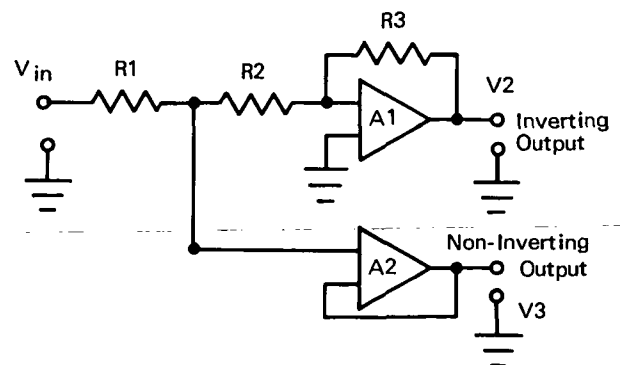
Circle 14 on Reader Service Card.

Section 4. Buffer and Isolation Amplifiers

BUFFER AMPLIFIER PROVIDES INVERTED AND NON-INVERTED OUTPUTS

A general purpose buffer amplifier, shown in the figure, provides both inverted and non-inverted output signals from a single input. The two outputs are proportional to the input, or if need be, can be varied to suit the application. Similar components in the inverting and non-inverting stages eliminate the adverse effects of component changes caused by temperature and aging.

In operation, A1 is connected as an inverting amplifier in a standard feedback configuration. A virtual ground in the feedback loop enables the output, V2, to act as a low im-



pedance. A2 is connected as a non-inverting unity gain amplifier in a feedback configuration which also provides a low impedance output.

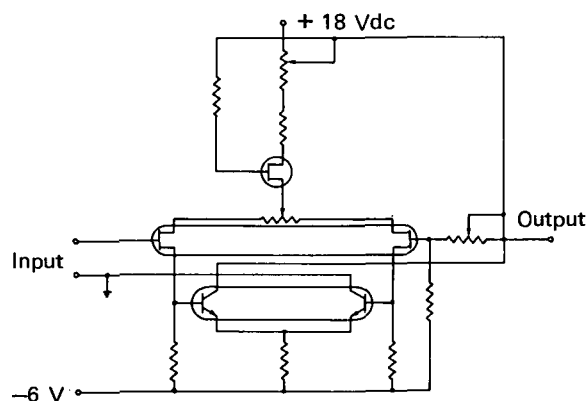
One important feature is the accurate tracking of the two outputs. This is achieved by having R1 and R2 common to both amplifier gains so that any variations will affect both outputs equally.

Source: C. A. Berard, Jr. of
Radio Corp. of America
under contract to
Goddard Space Flight Center
(GSC-11124)

Circle 15 on Reader Service Card.

FIELD EFFECT TRANSISTORS IMPROVE BUFFER AMPLIFIER

A unity gain buffer amplifier with a differential input stage has a faster response time than bipolar transistors when operated at low



current levels. The circuit shown in the schematic has an extremely high input impedance, low bias current requirements, and a wide bandwidth. A basic tradeoff between input current and bandwidth for optimum stability enables the amplifier to operate with an input bias current less than 10^{-8} A and a bandwidth greater than 2 MHz. The offset temperature stability for these conditions is 5 mV at 358 K.

Source: Dynatronics, Inc.
under contract to
Marshall Space Flight Center
(MFS-00916)

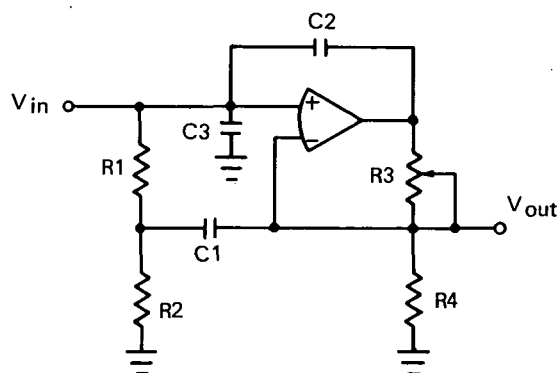
Circle 16 on Reader Service Card.

AC-COUPLED ULTRAHIGH INPUT IMPEDANCE AMPLIFIER

High input impedance and low input capacitance are achieved with a unity gain buffer amplifier having positive feedback. The circuit shown in the figure has an input impedance of several hundred megohms and input capacitance less than 1.0 pF.

The high input impedance is obtained by positive feedback through C1 to the positive input of the amplifier. The input capacitance plus the capacitance to ground can be cancelled by adding the feedback capacitor C2 and adjusting R3.

Since the low frequency response is determined primarily by C1, the use of an electrolytic



capacitor is advisable. High frequency response is limited by the operational amplifier. Using a μ a 709 amplifier, the circuit can amplify a 5 μ sec wide pulse coupled through a 1.0 pF capacitor.

Source: A. G. Birchenough
Lewis Research Center
(LEW-11154)

No further documentation is available.

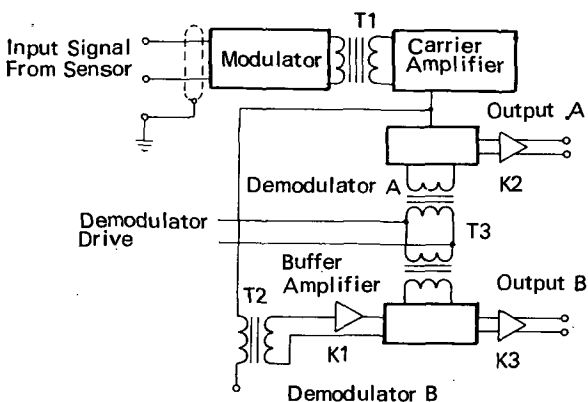
AMPLIFIER PROVIDES DUAL OUTPUTS FROM A SINGLE SOURCE WITH COMPLETE ISOLATION

An amplifier provides two outputs from a single input signal. Complete isolation from input to output is obtained and the two outputs can be grounded at different potentials. In typical use, one output is employed as a control signal while the second output provides signal monitoring. Adaptations of this method for achieving dual isolated outputs may be used in devices other than amplifiers.

A low-level signal from a basic sensor such as a thermocouple or strain gage is fed into differential input terminals of the amplifier through a twin conductor shielded cable. The signal is modulated to achieve an equivalent dc signal which is then coupled into a carrier amplifier via isolation transformer T1. After amplification to the desired level, the signal from the carrier amplifier is fed into output demodulator A for conversion back to an amplified duplication of the original signal. The carrier amplifier signal is also fed into demodulator B. In this path, however, transformer T2 and buffer amplifier K1 are added ahead of the demodulator. Transformer T2 provides carrier signal isolation and buffer amplifier K1 provides impedance isolation to prevent demodulator B from introducing spikes back into transformer T2.

Both demodulators, A and B, are simultaneously driven through separate isolated windings of transformer T3. Output amplifiers K2 and

K3 are included to provide low output impedance characteristics and load driving capability. No conductive paths exist between the



input terminals and output A, between the input terminals and output B, or between output A and output B. The ground voltage level is limited only by the breakdown voltages of the transformers, which can be controlled at the time of transformer production.

Source: C. R. Dipple of
Westinghouse Astronuclear Laboratory
and G. A. Neff of
Neff Instrument Corporation
under contract to
Space Nuclear Systems Office
(NUC-10056)

Circle 17 on Reader Service Card.

SIGNAL CONDITIONER, ISOLATION ATTENUATOR

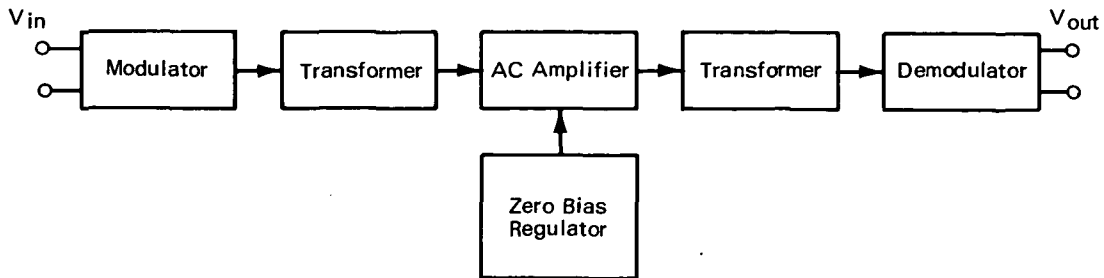
The isolation attenuator signal conditioner (see diagram) amplifies a positive dc low-frequency signal input and provides isolation between the input and output. The dc input

signal is first modulated (at the carrier frequency of 2.2 kHz) with a square wave reference signal of 7.5 V p-p.

The output, an amplitude-modulated square

wave, is transformer coupled to the ac amplifier. The ac amplifier includes an emitter follower input stage which drives the first of

arm of the potentiometer is capacitively connected to an input of the ac amplifier so that either positive or negative potentials can be



three differential amplifier stages. Series feedback and summing are employed within the amplifier for stability and control of the modulated signal. The input modulated signal and feedback signal are combined to produce an error signal that is amplified and transformer-coupled to the demodulator. The demodulator is driven in synchronism with the modulator. The resultant pulsating dc signal is fed to a simple RC filter network, employing a zener-diode network that limits the peak values of the output signal. The zero-bias circuit cancels any offsets which might occur in the modulator or amplifier. Two zener-regulated voltages of opposite polarity are connected to the ends of a 20,000 Ω potentiometer. The

selected. In addition, an integrated chopper transistor is connected, emitter to emitter, between the potentiometer arm and the converter ground. The chopper transistor is driven in synchronism with the modulator and demodulator. In this way, either positive or negative square waves of variable amplitude are injected into the ac amplifier input. This enables the dc amplifier signal output to be adjusted for null when the input signal is zero.

Source: G. Broxton of
 North American Rockwell Corp.
 under contract to
 Manned Spacecraft Center
 (MSC-15291)

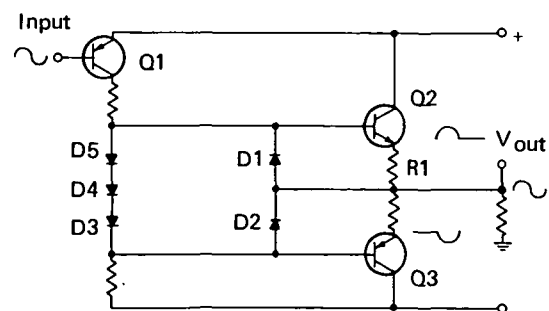
Circle 18 on Reader Service Card.

Section 5. Amplifier Circuits for Increased Reliability

CIRCUIT PROVIDES OVERCURRENT PROTECTION TO PUSH-PULL AMPLIFIER

The amplifier circuit shown in the figure limits the current output to a predetermined level. This limiting action protects the push-pull amplifier if the load is short circuited for any reason. If an excess current through R1 causes the voltage across it to equal the sum of the diode voltages D3, D4, and D5, the circuit starts to limit the current to a value determined by the value of R1.

If Q2 tends to draw excessive current, D2 turns on and applies a voltage across the emitter-base junction of Q3, opposite in polarity



to that required to maintain Q3 in the conduction state. Conversely, should Q3 tend to draw

excessive current, equal and opposite action would take place in D1 and the emitter-base junction of Q2, causing Q2 to turn off. Thus, no high frequency oscillation or driving voltage can cause both Q2 and Q3 to conduct at the same time, thereby short-circuiting the voltage across the two output terminals.

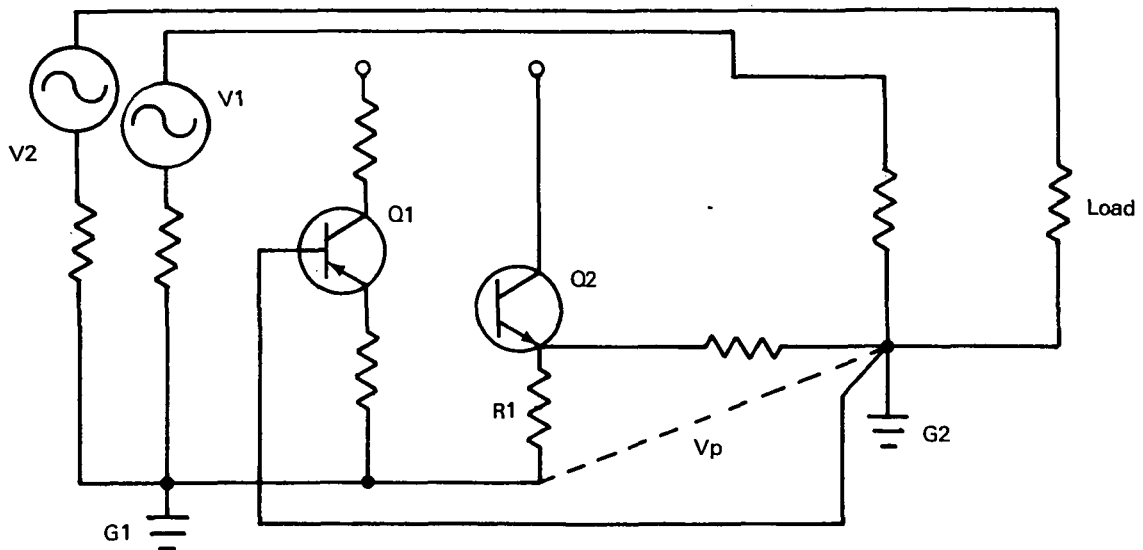
Source: D. J. Skorra of
Honeywell, Inc.
under contract to
Manned Spacecraft Center
(MSC-12033)

Circle 19 on Reader Service Card.

GROUND EQUALIZER AMPLIFIER

In many electronic systems, both ac and dc potentials exist between grounds of various parts of the system. The dc portion is generally

the ac current with no signal input; R1 is kept very small to minimize the input power requirement. To prevent noise frequencies from appear-



of little consequence, but the ac component can induce noise and errors into the system. In the circuit shown in the figure, the ground voltage is fed into an amplifier and returned to ground as negative feedback, thereby reducing the ground voltage essentially to zero. The amplifier senses the voltage drop (V_p) between G1 and G2 and produces a voltage rise approximately equal to V_p in the ground return. This voltage rise is in phase with the excitation voltages, V1 and V2, but as far as input-output relationships, the amplifier has an output which is in phase with the input.

Transistor Q2 carries a dc current equal to

ing in the ground circuit, the amplifier must have a high frequency response and must be decoupled above its effective frequency band with a suitable capacitor. For optimum operation, the signal returns should be grouped in each assembly, and the composite grounds should then be brought to the same potential by means of a single amplifier.

Source: K. James of
General Motors Corp.
under contract to
Manned Spacecraft Center
(MSC-12058)

Circle 20 on Reader Service Card.

CONTINUOUS REDUNDANCY DC AMPLIFIERS

The continuous redundancy technique, shown in the figure, for dc amplifiers greatly increases reliability in linear electronic systems. Previously, redundancy techniques have had such disadvantages as: double the power requirements, an increase in weight and space requirements, and a reduction in circuit gain upon failure of either circuit.

In this arrangement the functional block amplifier, made up of "n" parallel amplifiers, acts as a single amplifier. All but one of the amplifiers may be considered redundant. The sum of the outputs is used for feedback, so that a failure will result in increased outputs from the remaining amplifiers.

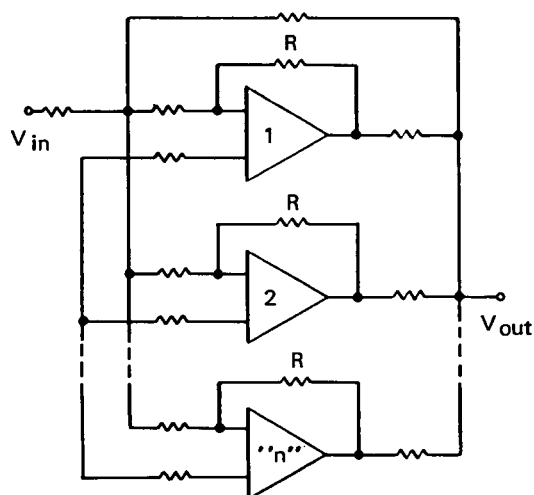
The most common and serious failure for any amplifier is opening or shorting of the B+

supply voltage. A short to B+ in a nonredundant system generally causes complete loop failure. In the redundant amplifier, however, the other paralleled amplifiers cancel out the effects of the shorted amplifier. The outputs of all the individual amplifiers are summed to provide a single common output. The gain of each individual amplifier should be as large as possible, with the only limitation on the value being the necessity of keeping the outputs of each stage as close to zero as possible for a zero-volt input.

The dynamic range of the amplifier, however, is reduced by 3.75 volts. This reduced dynamic range is the result of changing the output of each working amplifier in order to correct for the error voltage. If the normal dynamic range was 10 volts, it would be reduced to 6.25 volts by one failure. The useful dynamic range would be less than 6 volts, thus insuring that the full linear mode would be maintained.

This type of continuous redundancy applied to dc amplifiers is superior to previous standby techniques in that the redundant amplifier suffers only reduced dynamic range and increased offset. The gain and the phase response of the redundant amplifiers are not affected by a failure condition.

Source: F. C. Wellman
Marshall Space Flight Center
(MFS-12473)



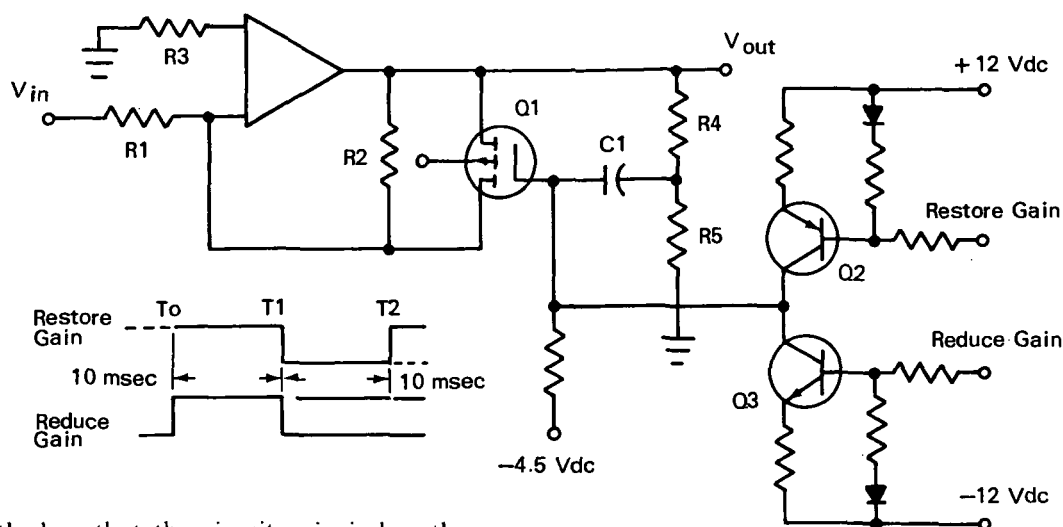
Circle 21 on Reader Service Card.

AMPLIFIER GAIN CONTROL

An amplifier gain control has been developed to reduce amplitude rise and fall times so that circuits which malfunction with fast rise signals can be operated correctly without exposure to sudden large signals. The circuit shown in the schematic reduces the amplifier gain, upon command, from unity to a minimum value and back to unity, in a quasi-linear fashion, in a time period from 3 to 10 msec.

Initially, C1 is charged to -4.5V, which biases

Q1 close to its conducting state. The reduce-gain control inputs are open so that Q2 and Q3 are off. Since R1 and R2 are equal, and Q1 is non-conducting, the signal output equals the signal input; i.e., the gain is one. At the reduce-gain control is grounded, causing Q3 to provide a constant charging current to C1. The voltage across C1 gradually increases, turning on A1 to increase the feedback and reduce the gain. At a time near T1, the resistance of Q1 is



sufficiently low that the circuit gain is less than 0.1 of the original value. At T1, the reduce-gain control is opened and the restore-gain control is grounded, turning Q3 off and Q2 on. Q2 provides a constant current discharge path for C1 and reverses the sequence. At time T2, Q1 is turned off and the original conditions are restored. R4 and R5 provide a reference point of one-half the signal to avoid unequal starting points when the signal is positive or negative.

Source: J. E. Goodwin, R. O. Leighou, and J. McGowan of Martin-Marietta Corp. under contract to Marshall Space Flight Center (MFS-14353)

Circle 22 on Reader Service Card.

SELF-CHECK CIRCUITS FOR AC AND DC AMPLIFIERS

Redundant monolithic operational amplifiers can be used to increase the reliability of electronic systems without an extensive increase in size, weight, and number of components. The dynamic self-test circuits shown in the figures are designed to checkout and evaluate operational amplifiers, with the aid of digital processing equipment. The self-test circuits can accept digital input commands and transmit output data without interfering with normal system operation.

AC amplifiers can be tested with the frequency detection scheme shown in Figure 1. Upon receipt of a digital command, a test-frequency input is applied to A1 and A2. The outputs from both amplifiers contain the test frequency with the same amplitude but phase

shifted π rad (180°). Since the test frequency signals from both amplifiers cancel when combined, the output from the summing amplifier does not contain the test frequency, and system operation is neither affected nor interrupted during the test procedure. If either amplifier fails, the test signal does not appear at A2.

A filter monitors the output of A2 and passes only the test frequency. The output of this filter feeds a comparator whose output (3V logic level) is applied to the digital data acquisition system for further evaluation.

Each dc amplifier in the redundant circuit may be tested using the level detection scheme in Figure 2. Upon receipt of digital test command, an FET switch applies a saturation signal to the amplifier under test. A comparator senses

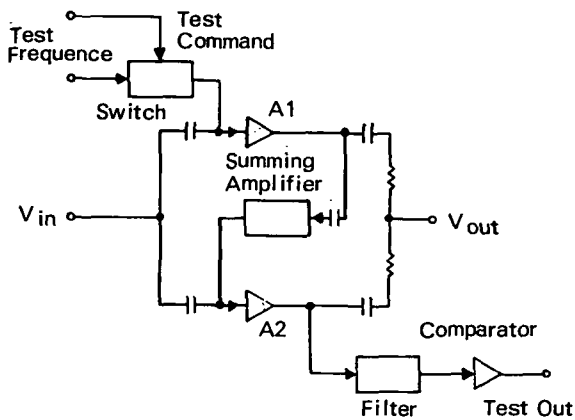


Figure 1A

the amplifier output and initiates a control pulse if the amplifier is functioning properly. Because only one amplifier is tested at a time, the other amplifiers are not disturbed and normal system operation continues.

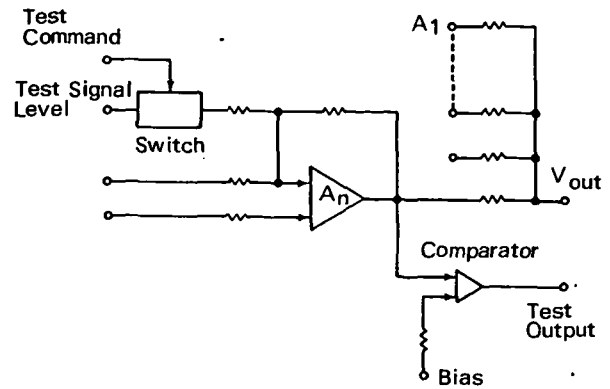


Figure 1B

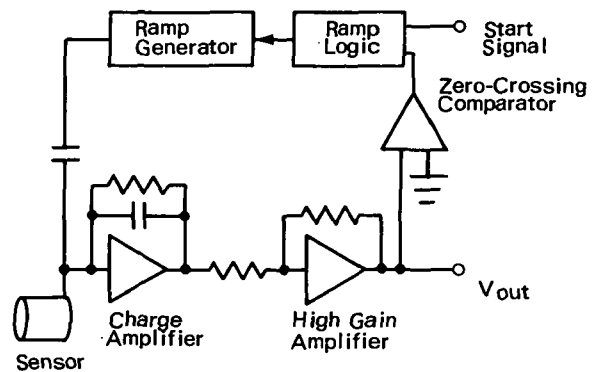
Source: F. C. Wellman of
Sperry Rand Corp.
under contract to
Marshall Space Flight Center
(MFS-12474)

No further documentation is available.

AMPLIFIER CORRECTS ERRORS INTRODUCED BY LARGE SPURIOUS INPUT SIGNALS

The amplifier circuit shown in the figure eliminates significant measurement errors which occur as a consequence of large spurious input signals. The shift in the reference baseline as a result of a large input signal prevents accurate measurement of the small signals which are intended to be measured. The solution to this problem, which is common to such instruments as nuclear particle detectors, is achieved by the novel technique of applying a signal of opposite polarity to correct the baseline shift. The charge amplifier senses the amount by which the reference baseline is shifted and applies the proper signal to a high gain amplifier. The output of the amplifier is returned to a control circuit which shifts the baseline to its proper level. As a result, a very small signal can be measured even after a large spurious signal is applied to the input.

The control circuit contains a zero crossing comparator which causes the residual



correction charge to be removed as soon as the baseline is returned to the original reference level.

Source: L. C. Labarthe of
Labko Scientific, Inc.
under contract to
Goddard Space Flight Center
(GSC-11016)

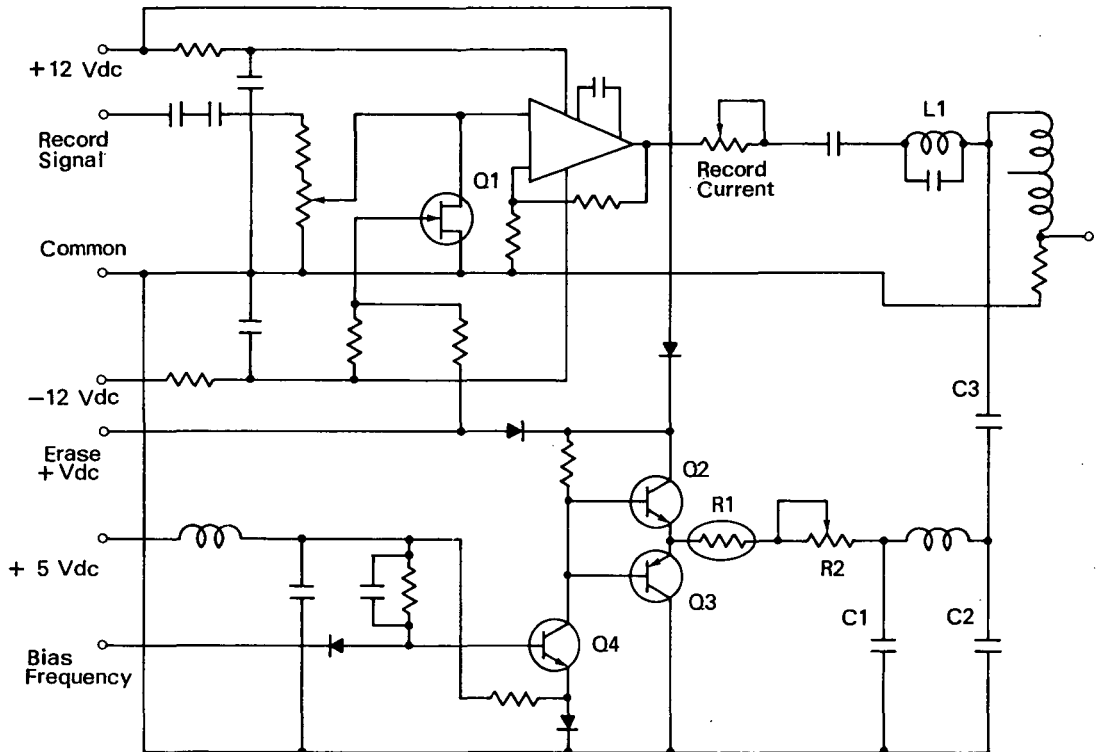
Circle 23 on Reader Service Card.

Section 6. General Purpose Amplifiers

LOW POWER BIAS AND ERASE CIRCUIT FOR MAGNETIC TAPE RECORDERS

A bias/erase circuit provides the necessary bias current for a group of modular, direct recording amplifiers. It also provides a simple means of erasing the tape using the same head as

During the half cycle when Q4 is turned on, Q2 is prevented from conducting, and the voltage at the emitters of Q2 and Q3 approaches zero. This quasi square wave is coupled through



that used for recording. An astable multivibrator generates a square wave signal which is applied to the bias frequency input of the record amplifiers. Each record amplifier contains a chopper amplifier, which switches between the dc supply and ground, to produce a square wave at the bias frequency. This square wave is then filtered to remove the harmonic content and is supplied to the record head as a low distortion current.

During normal recording, the square wave from the bias oscillator causes Q4 to turn on and off at the bias frequency of 400 Hz. When Q4 is off, the voltage at the emitters of Q2 and Q3 approaches the supply voltage (12 Vdc).

R1 and R2 to the filter, consisting of C1, C2, and L2, which removes the higher harmonics and provides a low distortion sine wave at the filter output. This waveform is coupled to the record head by means of C3, which is chosen to resonate with the record head inductance.

During the erase mode, circuit operation is essentially the same as that of the record cycle. The only difference is that 45 Vdc level is applied to the erase power input. With this higher input, Q2 and Q3 generate a 44 V p-p square wave voltage which increases the bias erase current in the head to a level sufficient to erase the tape completely.

The most notable features of the bias/erase circuit are: (1) good efficiency, because the amplifier transistors operate in a switching mode rather than as a linear amplifier; (2) amplitude stability is improved since it is primarily dependent on the value of the dc supply (normally well regulated); and (3) the bias oscillator can be a very simple relaxation oscillator. The only critical requirement is that it be reasonably close to a 50% duty-cycle square wave in

order to minimize the amount of second harmonic component.

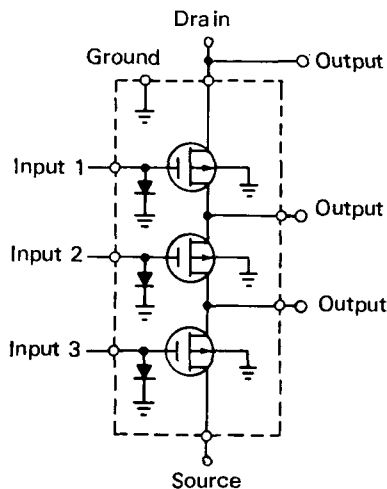
Source: A. E. Fisher of
Almond Instrument Co.
under contract to
Manned Spacecraft Center
(MSC-13808)

Circle 24 on Reader Service Card.

INPUT GATE CIRCUIT CONVERTED FOR USE AS A LINEAR AMPLIFIER

An input gate circuit containing MOS devices can be used as a linear amplifier. The 3-input NAND gate circuit shown in the figure

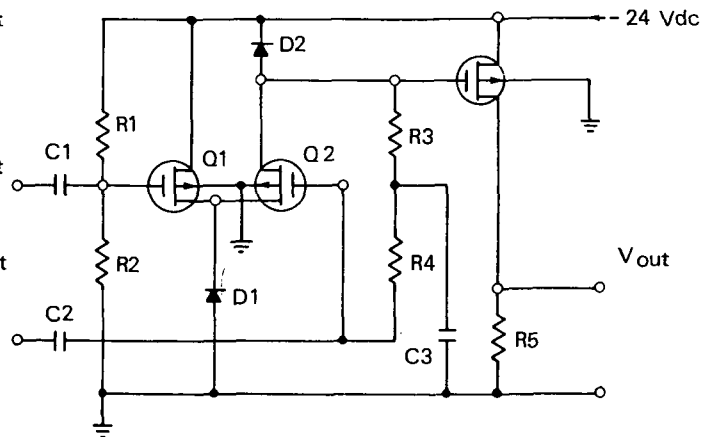
transconductance mismatch. The values of R1, R2, R3, and R4 are selected to balance the high input impedance ratios which are necessary for



MOS 3 Input Gate Circuit

contains the MOS transistors in series with the source and drain.

The ac input signal is coupled through C1 and C2 to the gate elements of Q1 and Q2, which form a differential amplifier. R1 and R2 form a voltage divider that provides the dc bias to Q1, and D1 supplies a constant current of 2 mA to the source elements of Q1 and Q2. The diode combination of D1 and D2 establishes the circuit balance regardless of temperature variations and also overcomes the problem of



Linear Amplifier Conversion

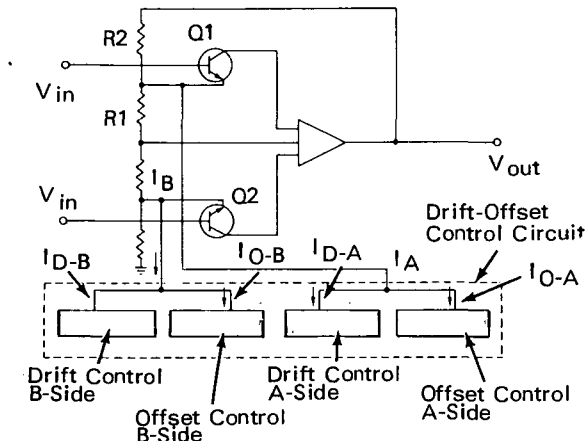
the MOS circuit operation. The important performance parameter is a voltage gain which is linear over a frequency range of 4 Hz to 100 kHz. Above 100 kHz, the gain decreases and is half-power at 180 kHz.

Source: T. P. Harper of
IBM
under contract to
Marshall Space Flight Center
(MFS-14265)

Circle 25 on Reader Service Card.

IMPROVED COMPENSATION CIRCUIT FOR DIRECT-COUPLED AMPLIFIERS

A novel control circuit, shown in the figure, compensates for the inherent temperature drift and offset of a closed-loop feedback amplifier. Disadvantages such as chopping spikes and the undesirable dynamic characteristics of conventional chopping circuits are minimized.



I_{O-A} and I_{O-B} : Temperature-Independent Currents

I_{D-A} and I_{D-B} : Linearly Temperature-Dependent Currents

The equivalent input voltage drift is less than $0.05 \mu\text{V/K}$ over the temperature range of 233 to 373 K. Power turn-on and overload settling are orders of magnitude faster than for chopping-type amplifiers. The circuit inherently allows monolithic integration of the entire amplifier in a 0.95 cm flat-pack.

Q1 and Q2 are the input transistors of the amplifier, and R1 and R2 form the emitter feedback network. Currents drawn from the R1-R2 nodes by the drift-offset control circuit compensate for the inherent temperature drift of the amplifier.

Note: Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to the TRW Space Technology Laboratories, One Space Park, Redondo Beach, CA 90278.

Source: D. R. Breurer of
TRW Space Technology Laboratories
under contract to
Manned Spacecraft Center
(MSC-11148 and 11235)

SIGNAL CONDITIONER, DC AMPLIFIER

The ability of this dc amplifier to accept input signals from 20 to 250 mV makes it ideally suited for signal conditioning applications in data acquisition and electronic test systems. The amplifier output, a maximum of 5 Vdc, is proportional to the input signal.

The simple circuit design permits the use of high-density packaging with a low-power consumption. Important circuit parameters include: reduced size; high input/output isolation (greater than 100 M Ω); an input resistance greater than 500 k Ω ; and a low output resistance less than 250 Ω .

As shown in the block diagram, the signal conditioner amplifier contains a modulator, an ac amplifier, dc-to-dc converter, and a demodulator with an output filter. The function of the full-wave modulator is to chop (or modulate),

at a 2.2 kHz rate, the signal applied to the input. The ac amplifier includes an emitter-follower input stage which drives the gain-setting attenuator circuit. The amplifier is succeeded by three differential amplifier stages, all direct-coupled, with the last one feeding the output emitter followers. Current supplied to the first differential stage provides a current feedback (depending on the common mode offset of the output emitter followers, which tends to keep both output emitter followers nominally biased at 4 Vdc. Additional degenerative feedback is incorporated throughout the amplifier stages to ensure stability.

The gain setting network, along with other critical gain controlling resistors, is contained within one unit in which all resistor temperature coefficients are matched to within 10 ppm/K.

property of high input impedance with very low drift and exceptional stability. The ability to operate the input stage at low collector currents, combined with the ability to select the transistors, decreases the noise figure below that of monolithic amplifiers.

The gain of the amplifier can be selected by changing the resistance ratio of R_4 and R_7 ,

and R_3 and R_6 . Limiting the bandwidth without affecting the common mode rejection of the overall amplifier circuit is accomplished by the addition of C_1 .

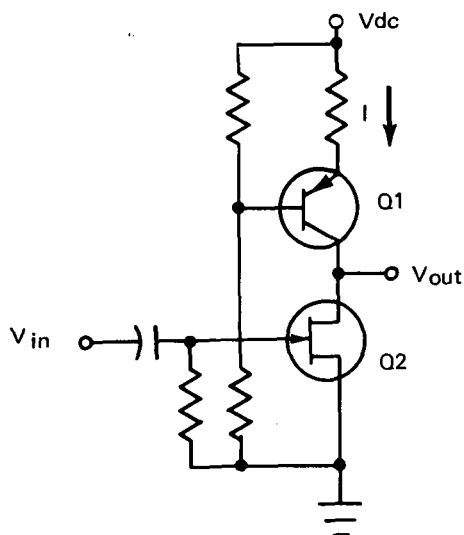
Source: J. Sturman
Lewis Research Center
(LEW-10712)

No further documentation is available.

GENERAL PURPOSE FET AMPLIFIER WITH HIGH GAIN AND LOW DISTORTION

High gain and low distortion are achieved with a simple FET amplifier that uses a current source as a load.

Most Class-A FET amplifiers operating with a load resistor have a gain equal to $g_m R$ where



g_m (mutual transconductance) is dependent upon the amount of current flowing through the FET. When a large ac input is applied, the current, I , varies inversely to the output signal. Therefore, the variation of g_m and the gain results in a distortion of the output waveform. The novel circuit shown in the figure reduces the distortion with the aid of a current source Q_2 that acts as the load impedance. The current source maintains I at a constant level, which in turn keeps g_m constant.

Other advantages obtained with this circuit include a higher gain factor and a reduction in power dissipation as a result of the smaller voltage drop across the current source.

Source: J. M. Fawcett of
Westinghouse Electric Corp.
under contract to
Manned Spacecraft Center
(MSC-13107)

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